First tests and equalisation studies of the TimePix 3 ASIC

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Resumo: O Timepix3 é um detector híbrido de pixels que está sendo utilizado como protótipo de estudos para o novo detector VELO upgrade que irá substituir o atual detector de micro tiras de silício no experimento LHCb no CERN. Em fase de desenvolvimento é crucial saber como o ASIC do detector responde sobre condições específicas para o desenvolvimento otimizado do chip VELOPix. Para garantir a boa qualidade dos dados adquiridos com o detector é necessário garantir que todos os pixels sejam eficientemente equalisados. Aqui será exposto o estudo sobre a equalisação do chip e a otimização dos parametros de equalisação.

Palavras-chave: LHCb, VELO, VELOPix, Timepix 3 ASIC.

Abstract: The Timepix3 is a hybrid pixel detector used as a prototype to studies for the new VELOPix detector that will replace the current silicon micro-strips VELO detector at the LHCb experiment. It is crucial to understand how the detector ASIC responds to specific working conditions for the development of the VELOPix chip. To assure a set of good quality data, all the pixels need to have an equalised response. We will show a study on the equalisation procedure and the optimization of its parameters.

Keywords: LHCb, VELO, VELOPix, Timepix 3 ASIC.

1. INTRODUCTION

The VELO (VErtex LOcator) is the LHCb's subdetector responsible for track and vertex reconstruction of the particles produced in the LHC collisions. Heavy hadrons are identified through their flight distance and hence the detector is critical for both the trigger and off-line physics analyses. The current VELO detector will change its detection technology from micro-strips to pixel detector and the Timepix3 ASIC (Application Specific Integrated Circuit) is currently used as a prototype version of the future VELOPix chip.

The Timepix3 chip is the successor of the Timepix [1]. The ASIC is comprises a matrix of 256x256 pixels of 55 μm pitch. Each pixel has its own and independent constructed analog and digital circuits with a 130 nm lithographic technology.

The main characteristic of the new chip is the ability to record the hit arrival time (ToA – Time of arrival) and deposited energy measurement (ToT – Time over threshold) simultaneously in each pixel, without dead time (for hit rates below $4x10^7$ hits/s/cm^2). A fast clock of 640 MHz provides a fine time resolution of approximately 1.6 ns.

The Timepix3 has a very similar architecture and characteristics, and almost identical analogue preamplifier, needed for the future VELOPix, it is of great interest for the LHCb collaboration to study and carefully characterize it.

The chip response can be sensitive to environmental condition changes, so it is important to know the best performance as a function of the parameters settings of the chip to make sure to have a good quality data set.

2. THE TIMEPIX 3 ASIC

2.1. The analog front-end

Each pixel analog front-end collects the charge generated by the ionizing particle passage through the sensor to the pixel electronics. The charge preamplifier has a Krummenacher feedback architecture with a discharge rate (I_{krum}) of the integrator capacitor. The dependence of the ToT with the input charge is ideally a linear function of I_{krum}.

The preamplified signal passes through a continuous-time discriminator with a 4-bit threshold adjusted by a current DAC. It is possible to control the effective threshold of each pixel individually to compensate pixel-to-pixel mismatches.

The discriminator output is fed to the digital part of the pixel. The discriminated rising and falling edges provide the ToA and ToT measurement. If a pixel is masked, the discriminator is disconnected from the digital circuit.

2.2. The digital front-end

Digital functionalities occupy most of the pixel area. The output from the amplifier goes to the Synchronizer and the clock gating, ruining at 40 MHz. Then it goes to counters and latches, where the digital information (ToA and ToT) from the analog amplified current is extracted. *Figure 1* shows a schematic visualization of how the TOT and TOA are measured.

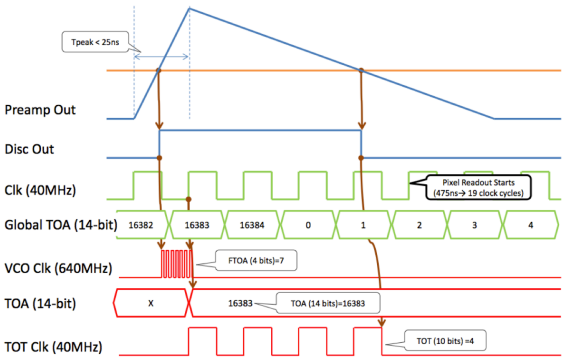


Figure 1: ToA and ToT graphic description

The ToT and ToA are recorded simultaneously in each pixel with 10 and 18 bits respectively. The ToA is measured using a 40 MHz clock for the most significant 14-bits. The additional 4-bits are measured with a 640 MHz local clock provided by the Voltage-Controlled Oscillator (VCO), shared by 8 pixels, which provides an additional resolution of 1.56 ns.

3. EQUALISATION

With over 65k pixels it is important to adjust them all in a way that different pixels have the same response for the same input charge, generated after a particle hit. The chip can be sensitive to environmental conditions, therefore it is important to equalise in between data taking periods.

Each pixel is equipped with a threshold equalisation DAC, which corrects for pixel-to-pixel mismatches. This 4-bit trim DAC is able to shift the effective global threshold and, therefore, can be used to compensate the threshold mismatches.

The global threshold scan is made over the electronic noise. It is reasonable to assume that it is constant and uniform over the pixel matrix, making all pixels have almost the same input charge.

3.1. Equalisation Method

Firstly, the test pulse is disabled for all pixels during the whole equalization procedure. The 4-bit trim of each pixel is adjusted to its lowest value, and a specific pixel mask layout (defined by the spacing between the pixels as showed in *figure 2*) is applied to avoid cross-talk feedback between the pixels. The threshold voltage is scanned from its lowest to its highest value and the number of noise hits is recorded for each threshold. After that he mask changes its position and the scan is repeated. This occurs n^2 times, where n is the spacing (in pixels) between the enabled pixels.

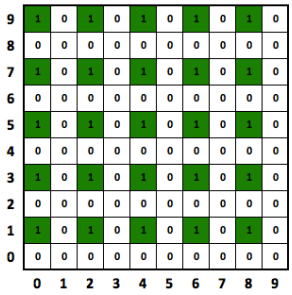


Figure 2: Pixel mask bits distribution for spacing 2

Once the scan is finished, the 4-bit trim is adjusted to its highest value 0xF (1111) and the same routine is repeated.

After the two threshold scans is done it is possible to interpolate the trim values and the best 4-bit adjustment of the local threshold for each pixel is extracted. The global threshold voltage scan is performed again to assess the quality of the equalisation. The typical results are shown in *figure 3 and 4*.

A final plot can be made to show the matrix final state. It is a histogram that shows how many pixels sees an event per threshold. As expected, it is possible to see that when the matrix is unequalised, each pixel sees the electric noise (uniform over the matrix) at different global threshold levels. When the pixel matrix is equalised, all the pixels reach the noise level with approximately the same global threshold. The graph can be seen on figure 10. In blue is the pixel distribution when configured with the 4-bit 0x0. In red, is shown the distribution for 4-bit equal to 0xF and in black is the distribution for the equalised matrix.

3.2. Optimization of equalisation parameters

The pixel spacing is a parameter that has major influence on the equalisation is. It is important to quantify the difference between spacings to know the best spacing that yields to a good equalisation without taking too much valuable time (once it goes with the square of the spacing).

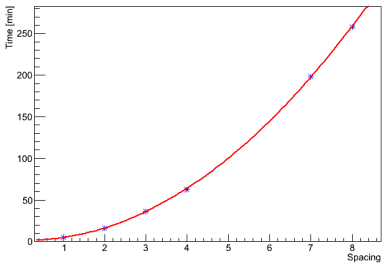
The equalisation performance can be quantified looking for the RMS of the final pixel distribution over the threshold scan. A good equalisation will yield to a smaller RMS.

The other parameters ware the current I_{krum} as it has a major role on the analog performance, and the duration of the acquisition time (length of the shutter).

3.3. RESULTS

3.3.1. Spacing

As expected, the time to perform the full equalisation goes with the square of the spacing,



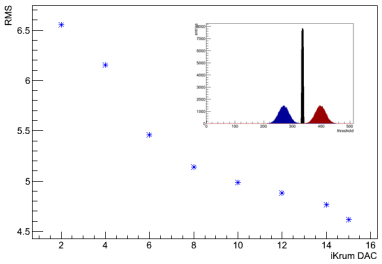
once it has to move the mask along the matrix in the two dimensions. With spacing 4 the equalisation took around 60 minutes.

The spacing has also changed the event count over the threshold scan, making the threshold spread get narrower with higher spacings. This could be explained by a cross-talk between pixels which decays with the distance between the enabled pixels. See *figure 12*.

As the noisy threshold spread was getting narrower, the distribution of the pixels counting over the threshold got wider (by a factor of 10%) with increasing spacing. This effect is probably due to a positive-feedback (one pixel generating signal on a neighboring pixel), which also appeared in the spacing scan.

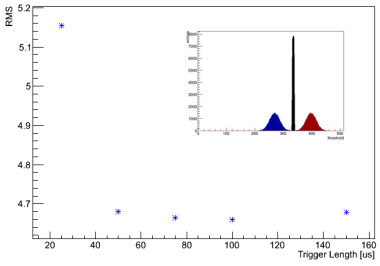
3.3.2. I_{krum}

The I_{krum} controls the discharge rate of the feedback capacitor. It affects the time-to-peak of the front-end preamplifier that should be of the order of 25 ns, in order to yield a sufficiently low timewalk and match the LHCb applications. The RMS of the equalisation pixel distribution gets lower with increasing the Ikrum setting as shown F*igure 14.*



3.3.3. Shutter Length

The last parameter tested was the shutter frame time, or how long is the acquisition time. It rapidly stabilizes to its stable value, which allows the chip to perform more/other tasks faster. F*igure 15* shows the RMS as a function of the



trigger length.

5. CONCLUSION

The Timepix3 is a new ASIC that shows a good preliminary performance. An equalisation algorithm for the pixels was checked and many tests of the equalisation performance were made. A set of optimal equalisation settings is proposed and future applications are expected.

7. REFERENCES

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