Clock-Less Analog-to-Digital Converter

Sabiniano A. Rodrigues[1,2,3], Hassan Aboushady[2], Marie-Minerve Louërat[2], José I. C. Accioly[1] and Raimundo C. S. Freire[3]
[1] Federal Institute of Education Science and Technology of Paraiba (IFPB), João Pessoa – PB, Brazil
[2] University Pierre & Marie Curie (Paris VI), LIP6 Laboratory, 75252 Paris, France
[3] Federal University of Campina Grande (UFCG), CEEI/LIMC Laboratory, Campina Grande – PB, Brazil

***Abstract*—This article presents a new clock-less analog-to-digital converter (ADC) based on a full analog signal processing. The main innovative feature of the proposed ADC is that, for a sampled input signal, a cascade of identical stages may operate without timing signal (clock) with its analog processing independent of the output digital signal's generation. Clock-less converters are used in the medical area, in control equipment, and portable equipment of low consumption. In this work, time of conversion of 0.5 µs was obtained by simulations with spice macromodels, for a converter of 8 bits resolution, with 8 mW consumption. The Signal-to-Noise Ratio (SNR) reaches 60 dB.**

***Index Terms* – Analog-to-Digital Converter (ADC), Analog Signal Processing, Asynchronous, Analog, Irregular Sampling, CMOS.**

I. INTRODUCTION

Clocked processors have dominated the computer industry since the 1960s because chip designers saw them as more reliable, capable of higher performance, and easier to design, test, and run than their clock-less counterparts. The clock establishes a timing constraint within which all chip elements must work, and constraints can make design easier by reducing the number of control decisions [1].

In synchronous designs, the data moves on every clock edge, causing voltage spikes. In clock-less chips, data are not all produced at the same time, which spreads out current flow, thereby minimizing the strength and frequency of spikes and emitting less electromagnetic interference (EMI). Less EMI reduces both noise-related errors within circuits and interference with nearby devices [1].

Because asynchronous chips have no clock and each circuit powers up only when used, asynchronous processors use less energy than synchronous chips by providing only the voltage necessary for a particular operation [1].

Analog-to-digital converters (ADCs) are usually specified to have a fixed conversion time, but clock-less ADCs is gaining relevance in many fields, ranging from astronomy to medicine. Some applications in equipment of the medical area, such as X-rays and spectrometry equipments, need ADCs that are activated by the beginning of the event and closed down in the end, to control the energy sent during the event. Thus, the conversion time has a large rang of variations [2].

Another possible application of clock-less ADC is in wireless net data and web applications components. The new equipment generation for wireless nets imposed a significant change in the converting data circuits. These systems must be low-cost, reduced-size, low-noise, and, especially low-power because they are frequently powered by batteries or remotely powered [3,4].

Moreover, some works show that continuous-time digital signal processing is possible, and that it presents several advantages in comparison to the classical, discrete-time case: no signal aliasing and no quantization error aliasing. This avoids sub-harmonic components, and reduces the in-band quantization error power [5].

This work presents a converter with analog processing, which increases the immunity to noise.

This paper is organized as follows. After this introduction, Section II presents the basic concept of the conversion technique. Section III gives details about the ADC behavior. In the Section IV simulations results are reported. Section V concludes the paper.

II. BASIC CONCEPT OF THE CONVERSION TECHNIQUE

The general architecture of the proposed clock-less ADC is shown in Fig. 1. This structure has similarities with the structure of a standard pipeline ADC.

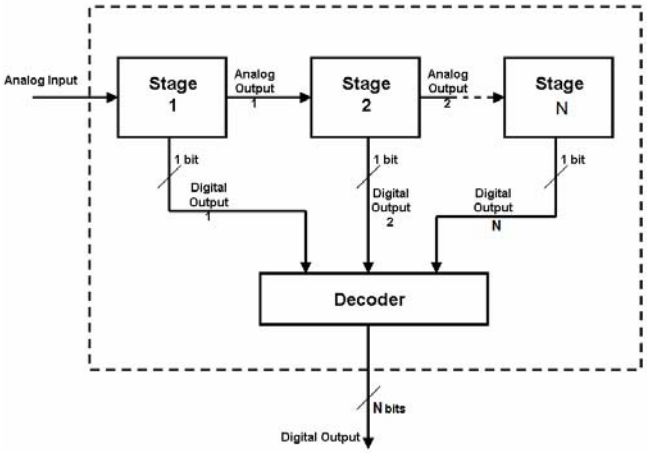

Figure 1 – Block diagram of the ADC

In order to explain the behavior of the clock-less ADC, an architecture of 3 bits is presented in the following.

It consists of three conversion stages and one decoder (array of logic gates) (Fig.1). The algorithm of one stage is shown in Fig. 2.

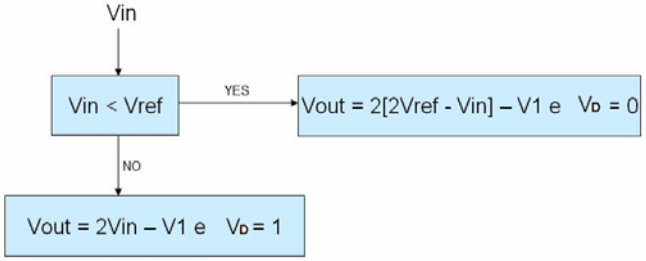

Figure 2 – Conversion algorithm of one stage

A pipeline converter consists of a cascade of identical stages that are separated by a sample-and-hold amplifier . This sample-and-hold amplifier is part of the sub-converter stage [6].

The clockless ADC consists, also, of a cascade of identical stages, but without sample-and-hold separating them. Each stage provides one bit of partial conversion. The output bits of each one of the stages are converted by a decoder to standard binary code.

The schematic diagram of one of the stages is shown in Fig. 3.

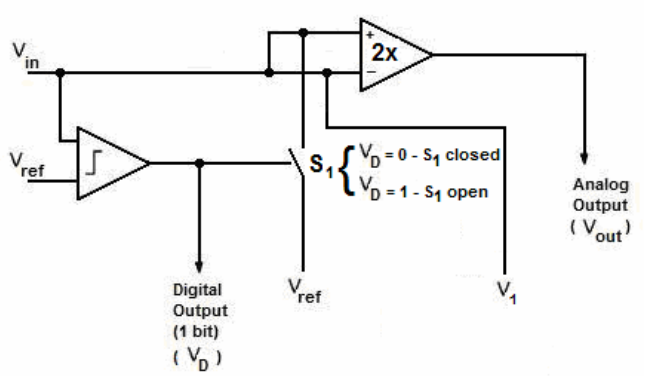

Figure 3 – Schematic diagram of one stage

Thus, the output voltage of each stage of the clock-less ADC is as follows:

$$V_{out} = 2 * [2 * V_{ref} * \overline{V_D} - \overline{V_D} * V_{in} + V_D * V_{in}] \quad (1)$$

III. ADC BEHAVIOR

In the following the architecture of each stage is detailed.

Depending on the value of the output digital signal, the amplifier is set in two different configurations. The first one happens when Vin ≥ Vref. The digital output bit is 1. Switch S_1 is open and the output voltage becomes as follows:

$$V_{out} = 2 * V_{in} - V_1 \quad (2)$$

The peak value of the output analog signal is limited by voltage V_1.

Fig. 4 shows the circuit of the first configuration.

The second configuration happens when Vin < Vref. The digital output bit is 0. Switch S1 is closed and and the output voltage becomes as follows:

$$V_{out} = 2 * [2 * V_{ref} * \overline{V_D} - \overline{V_D} * V_{in}] - V_1 \quad (3)$$

Fig. 5 shows the circuit of the second configuration.

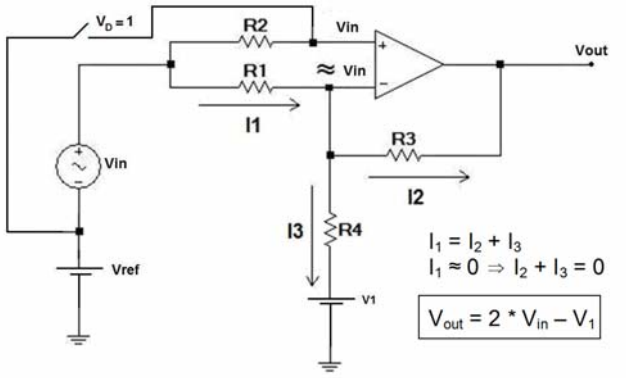

Figure 4 – First configuration of the amplifier

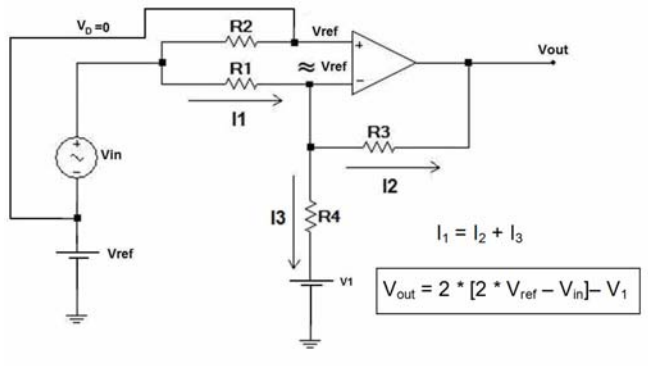

Figure 5 – Second configuration of the amplifier

In this clock-less ADC, the output digital signal only controls the switch that changes the configuration of the operational amplifier, whereas in pipeline ADC the digital signal is subtracted to the analog one.

Fig. 6 shows the input analog signal, the output analog signal and the output digital signal of the first block. This figure shows that in each point of comparison between the output analog signal and Vref, a transition is generated in the output digital signal.

Once the analog signal is processed by one stage, the frequency is doubled between input and output. This effect can be compared to the "folding" converters.

In this way the dynamic performance of the clock-less ADC is mostly determined by the performance of the operational amplifiers of the last stages.

The digital outputs provides a binary code different form the standard one. It has the advantage to present a unitary Hamming distance between its possible words.

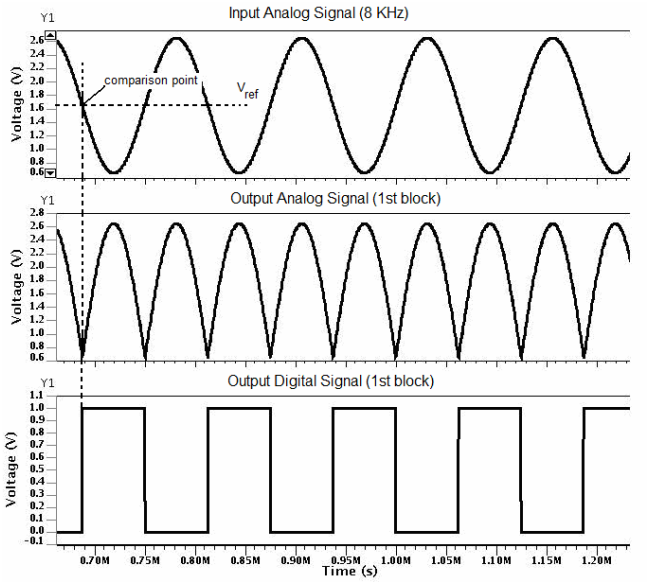

Figure 6 – 1.Input Analog Signal; 2. Output Analog Signal (1st stage); Output digital signal (1st stage).

The Hamming distance is used as parameter for optimization of circuits of data search in memory and error correcting codes in data transmission [7,8].

The 3 bit configuration is illustrated in Fig. 7. We can observe that never more than one transition of the digital signals arises at the same time.

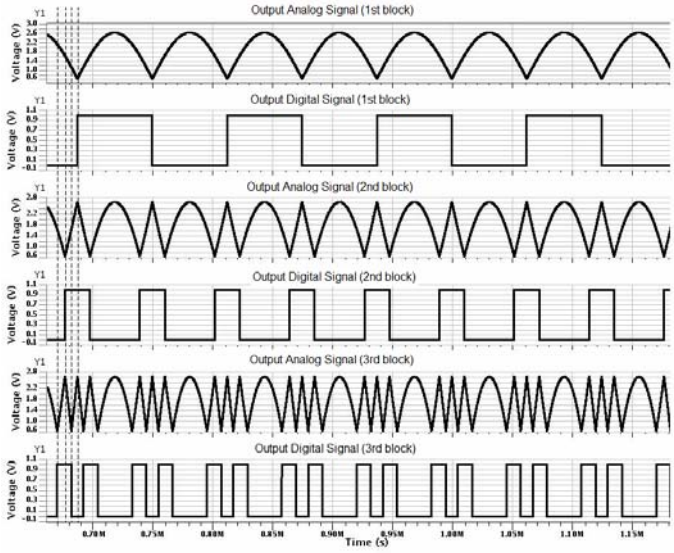

Figure 7 –Output Analog Signal and Output digital signal for the 1, 2 and 3 stages.

Therefore, to cope with converters digital-to-analog (DAC) standards, the output code of the ADC must be decoded to a standard binary code.

IV. Simulation Results

In this system an ideal signal level matching is assumed. In practical applications, however, timing and accuracy limitations can result in conversion problems resulting in "missing" codes. To avoid such a problem, the gain of the operational amplifiers is increased with respect to get the accurate values of voltage in the comparison points.

Simulations were made for the operational amplifiers to be sure that the value of the comparison points is not limited.

To find DC gain (A0) of the amplifier, the pole was fixed on 50 KHz and a variation of DC gain is made. To find product DC gain versus bandwidth (GBW), the DC gain was fixed on 80 dB and a variation of the pole is made.

The Fig. 8 shows the clock-less ADC SNR as a function of the gain of operational amplifier used. And the Fig. 9 shows the clock-less ADC SNR as a function of the product DC gain versus bandwidth (GBW).

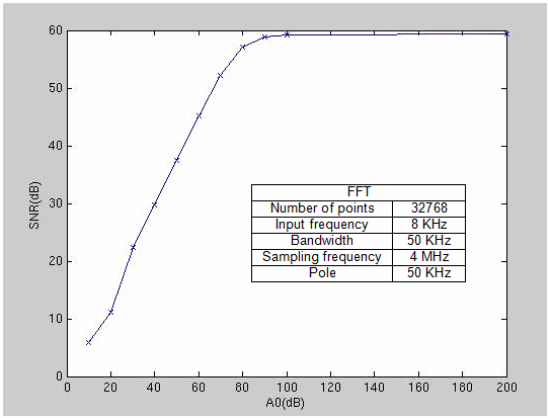

Figure 8 – Simulation DC Gain (amp.) x SNR (ADC).

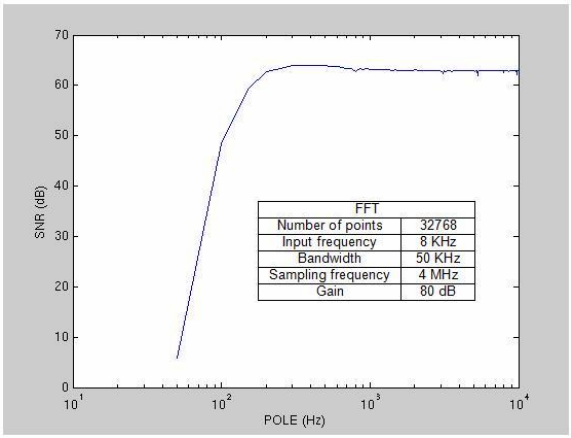

Figure 9 – Simulation Pole (amp.) x SNR (ADC).

These simulations indicated the possibility of working with an operational amplifier of 70 dB DC gain and 7.5 KHz pole.

For irregular sampling ADCs, $2^M - 1$ quantization levels are regularly disposed along the amplitude range of the signal. A sample is captured only when the analog input signal Vin crosses this level. In the clock-less ADC, only there is one level of comparison (Vref).

Contrary to classical Nyquist sampling, samples are not regularly spaced out in time, because it depends on the signal variation: the sharper the signal, the closer the samples.[9]

Then, the sampling frequency used in the calculation of the FFT was determined by the measurement of the smallest time of sampling, of the quantized output signal.

The figure 10 shows the difference between the maximum and minimum sampling times for um clock-less ADC of 3 bits.

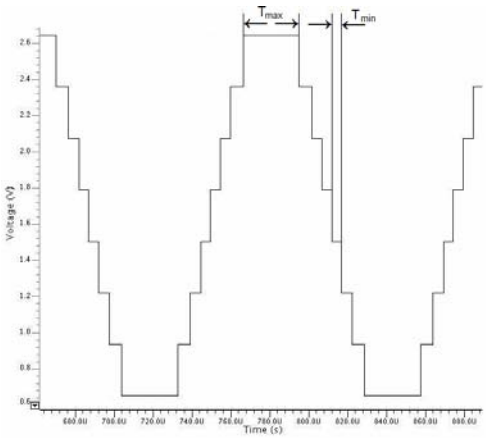

Figure 10 – Quantized signal in 3 bits for a sinusoidal signal of 8 KHz.

The simulations results are presented in table 2. These results were obtained by the Fast Fourier Transform (FFT) of signal, using the Matlab software. It was measured the smallest time for converting a sinusoidal signal of 8 KHz and used this time as the inverse of sampling frequency. The Fig. 11 shows the waveform of the FFT signal.

TABLE I. SIMULATIONS RESULTS OF CLOCK-LESS A/D CONVERTER

Items	Amounts
Input Frequency (fin)	8 KHz
Conversion time	≈ 0,5 µs
Bandwidth (BW)	50 KHz
DC Gain (amp.)	70 dB
GBW (amp.)	≈ 45 MHz
Resolution	8 bits
Power consumption	8 mW – 3,3 V
ENOB	≈ 9,7 bits
SNR	≈ 60 dB

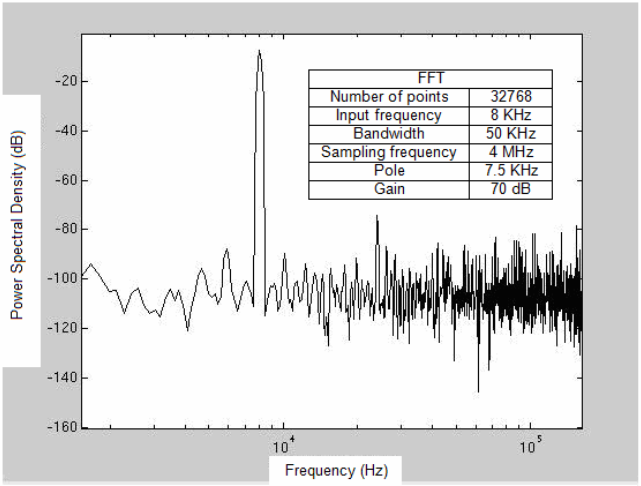

Figure 11 – FFT wave form of output signal generated by the proposed converter.

The Effective Number of Bits (ENOB) was calculated with the equation as follows:

$$ENOB = (SNR * 1.78)/6 \qquad (4)$$

V. CONCLUSION

In this paper, a new kind of A/D converter, clock-less, with full analog processing, is proposed. The main innovative feature of this ADC is that for being relatively independent, the generation of the output digital signal and the analog processing of the input signal, increases the speed of the converter compared to clock-less converters where the analog processing of the input signal is influenced by the result of conversion. The clock-less ADC converter with operational amplifier of 70 dB gain and 7.5 KHz pole, provides a conversion every 0.5 µs and consumes 8 mW from a 3.3 V power supply.

REFERENCES

[1] Geer, D., "Is It Time For Clockless Chips?", IEEE Computer Society, March 2005.

[2] Picolli, L., Rossini, A., Malcovati, P., Maloberti, F., Borghetti, F. and Baschirotto A., "A Clock-Less 10-bit Pipeline-Like A/D Converter for Self-Triggered Sensors", IEEE Journal of Solid-State Circuits, Vol. 43. No. 2, February 2008. [1]

[3] Arias, J., Boccuzzi, V., Quintanilla, L., Enríquez, L., Bisbal, D., Banu, M. and Barbolla, J., "Low-Power Pipeline ADC for Wireless LANs", IEEE Journal of Solid-State Circuits, Vol. 39. No. 8, august 2004.

[4] Tomohiko, I., Daisuke, K., Takeshi, U., Takafumi, Y., and Tetsuro, I., "55-mW, 1.2-V, 12-bit, 100-MSPS Pipeline ADCs for Wireless Receivers", IEICE Trans. Electron., Vol. E91-C, No. 6, June 2008.

[5] Tsividis, Y., "Digital Signal Processing In Continuous Time: A Possibility For Avoiding Aliasing And Reducing Quantization Error", ICASSP'04 IEEE International Conference on Acoustics, Speech, and Signal Processing, 17-21 May 2004, Montreal, Canada.

[6] R. van de Plassche, "CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters", 2nd ed., Boston, MA, Kluwer, 2003.

[7] Rodrigues, S.A., Accioly, J.I.C., Freire, R.C.S. and Pessoa I.M., "Asynchronous Analog-Discrete Converter Using An Analog Signal Processor Stabilized In An Inflection Point", 12th IMEKO TC1 & TC7 Joint Symposium on Man Science & Measurement, September, 2008, Annecy, France.

[8] Fung, F. Y. C., "A Survey of the Theory of Error-Correcting Codes", Harvard-Radcliff Math Bulletin, Vol.1 (1994).

[9] Allier, E., Sicard, G., Fesquet, L. and Renaudin, M., "A New Class of Asynchronous A/D Converters Based On Time Quantization", Proceedings of the Ninth International Symposium on Asynchronous Circuits and Systems (ASYNC'03)", May 2003, Vancouver, Canada.