CMOS A/D Converter for SOC in Wireless Sensor Network Applications

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Abstract: A cyclic 8-bit analog-to-digital converter with a 50kSamples/s sampling rate, embedded on a system on chip for wireless sensor network applications, was developed. The IC was designed and prototyped. Its analog and digital cores were successfully characterized.

Keywords: A/D Converter, System on Chip, Wireless Sensor Network, Integrated Circuit.

1. INTRODUCTION

A CMOS system on chip (SoC) for wireless sensor network applications is being developed at Universidade de Brasília (UnB). The integrated circuit comprises a digital processor, a 900 MHz RF transceiver, an analog data acquisition interface, a digital serial interface and an embedded memory module. Possible applications include animal and vegetable tracking, environment monitoring, precision agriculture and industrial process monitoring. In this work, an analog-to-digital converter (ADC) that will be included in this SoC, is presented.

Considering the applications mentioned above, the SoC must be cheap and present reduced power consumption. The cost of the SoC can be reduced by using a conservative fabrication process, 0.35u CMOS in our case, and small silicon area. The power consumption of the system can be reduced by intelligent power management techniques, such as keeping the chip on an idle state when its main functionalities are not required. Low power/low voltage design is not being used in order to simplify the overall design flow.

The ADC was implemented using a cyclic architecture. In this kind of circuit, a small set of basic cells performs repetitive simple analog operations over an input signal to progressively compose an equivalent digital word that represents that signal. This scheme allows a favorable trade-off between performance, power consumption, chip area and design simplicity when compared to other classic ADC architectures [1][2].

This paper outline is as follows. Section 2 presents the ADC overall architecture. In Section 3, the design flow is presented. Section 4 brings results and discussions about the ADC. Finally, Section 5 presents conclusions and shows future trends in the design of wireless sensor networks.

2. ADC ARCHITECTURE

A cyclic ADC is a mixed-signal circuit that implements an algorithm to convert an analog value to its digital counterpart. The algorithm implemented by the proposed ADC is shown in Figure 1. In this algorithm, the input signal S is compared with zero. If S is positive, the output is set to logical one, then S is doubled and subtracted from the reference value M. If S is negative, the output becomes logical zero, S is doubled and summed with M. This cycle is repeated until the desired number of bits is obtained.

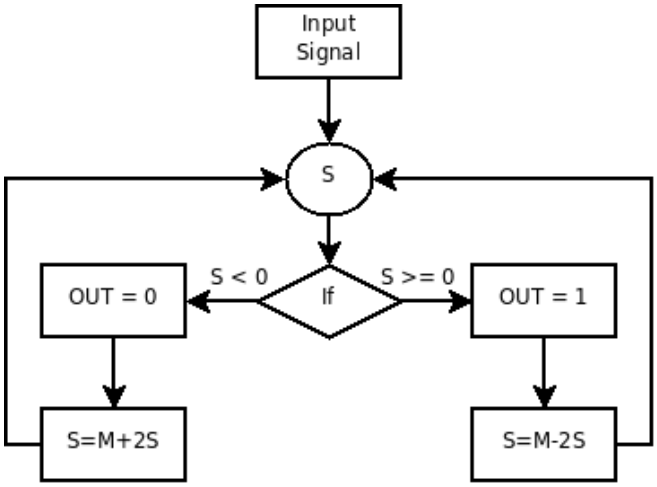

Figure 1. Algorithm implemented by the proposed ADC.

In switched-capacitor circuits, mismatching between the components of the circuit increase error in conversion. Many schemes were proposed to avoid this problem, but the final circuit complexity is always increased. As one of the goals of this work is to maintain simplicity, a switched-current architecture was chosen [3][4].

The described algorithm has been implemented using three basic analog blocks: current copy cells, a current comparator and several switches. The summing operations can be easily done by wiring two current sources to the same node. A block diagram of the proposed ADC is shown in Figure 2.

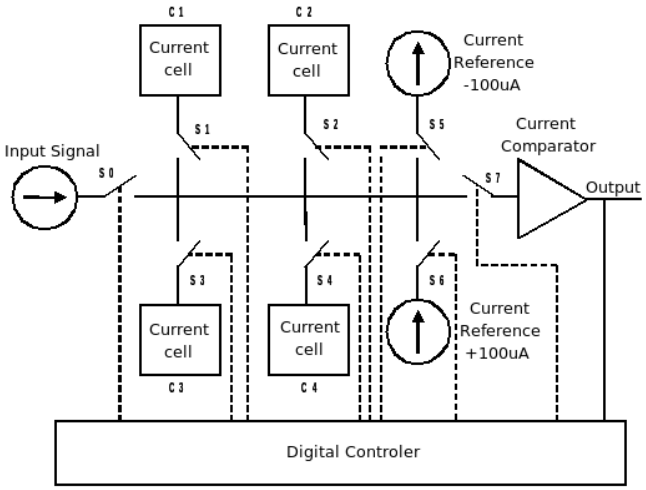

Figure 2. Schematic view of the designed ADC.

The ADC operation is as follows: 0) All the analog switches are open in the beginning of conversion. 1) S0 and S7 are closed and the current comparator outputs the first bit. 2) S7 is opened while S0 and S1 are closed, making the current signal to be copied into the cell C1. 3) S1 is opened and S2 is closed, copying the input signal into the cell C2. 4) S0 is opened while S1, S2 and S7 are closed. One of the keys S5 or S6 are also closed depending on the previous output bit, making the comparator output the next bit. 5) Switch S7 is opened and S3 is closed. This way, the appropriate current is copied into cell C3. 6) S3 is opened while S4 is closed, copying this current to cell C4. 7) To decide about the next bit, switches S1 and S2 are opened and S3, S4 and S7 are closed in addition to S5 or S6, depending on the previous output bit. In next states, currents are copied into cells C1 and C2, compared and copied back into cells C3 and C4. These operations are repeated until the desired number of bits is achieved.

3. ADC DESIGN

For SoC applications, it was specified that the ADC should work at 50kSamples/s and be able to handle signals up to 25kHz. Its output must be 8 bit long, with at least 7.5 effective bits. Its dynamic range should be from -100uA to +100uA.

The analog blocks of the circuit were designed using a full-custom design flow from specification to layout while the digital controller was described using VHDL language and later synthesized in a standard cell design flow [5]. To ensure correct circuit functionality, a mixed-signal simulation was performed after the design of the analog and digital cores.

Figure 3 shows the structure of a basic current cell [6]. In this basic block, the three terminal transistor M0 works as a switch controlled by the input *phase1*. The four terminal transistor M1 operates as a current source while the capacitor C0 stores an analog voltage value.

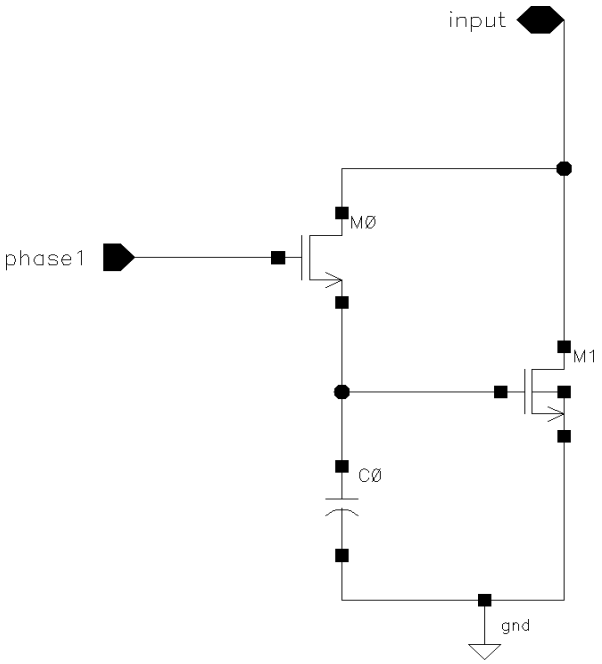

Figure 3. Basic current cell schematic.

This circuit has two work stages: a sampling stage and a hold one. In sampling stage, *phase1* voltage level must be logical one (close to VDD). This way, an input current can charge/discharge capacitor C0. As the capacitor voltage changes, the input current starts to flow only through transistor M1. In steady-state, the capacitor current will be zero and its charge will be sufficient to maintain the input current flowing through transistor M1. In hold stage, *phase1* input is logical zero (close to GND), isolating capacitor C0. This way, the current drained by transistor M1 will be weakly dependent on the input port voltage as long as transistor M1 is kept in saturation.

Since this cell is able to sink current, but not to supply it to an external circuit, a complementary block was added to the final ADC architecture in order to perform this function. Clock feedthrough reduction techniques were also adopted to minimize conversion errors in final circuit.

In the ADC input, a current sample-holder circuit was added, based on the current cell. As sensor signals change, error can be induced in conversion. This additional block minimizes this error source.

The current comparator was implemented as a simple voltage comparator with low impedance loads placed on its input pins as well as with off-set correction feedback.

The digital controller is a state machine in charge of controlling all the switches of the analog core. It also has to capture the output bits and interface with external devices.

4. RESULTS AND DISCUSSION

The proposed circuit was prototyped in a typical 0.35um CMOS process with other digital and RF circuits. Figure 4 shows a picture of the chip with ADC (block A) and its test structures (block B) highlighted.

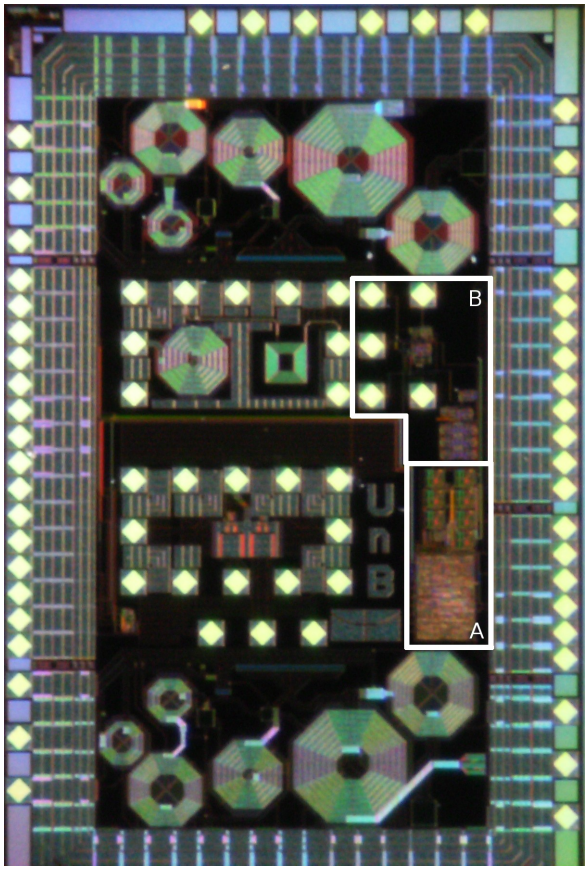

Figure 4. Die photography showing the ADC.

Design for testability techniques were used to improve the controllability and observability of the basic cells. The final area of the complete circuit was 0.3mm^2, equally divided between the analog core and the digital controller. In simulation, the circuit consumed approximately 2mW during normal operation.

An important parameter for this topology is its output impedance, since the output signal is a current. This impedance was designed to be greater than 50MΩ over the frequency range of interest, despite all fabrication process variations.

Figure 5 presents a mixed-signal simulation of the ADC. In this figure, the waveform A is the input current. During the conversion cycle, the input current is zero because the input switch is kept open. The waveform C shows the stored current after sampling. This is the current that will be used by the circuit to generate the 8-bit digital word. Waveform D shows the output bits in hexadecimal format.

A simulation of the digital controller is shown in Figure 6. This simulation was designed to cover many functions such as single conversion and 4 conversions in a row. In this figure, RD_Out shows the analog core switches control signals in a serial way, ConvDone indicates the final of a conversion cycle and RD_Out_Byte is the converted bits output (01010101 in this test case). Other internal signals are also shown.

Figure 7 shows the characterization results for this block obtained with a logic analyzer. The signals ROBYTE, CVDONE and RDOUT, which respectively correspond to RD_Out_Byte, ConvDone and RD_Out in Figure 6 were obtained as expected from the circuit, showing that the digital controller works as specified. The measured sampling rate was 50kSamples/s as well as the 8 bit resolution.

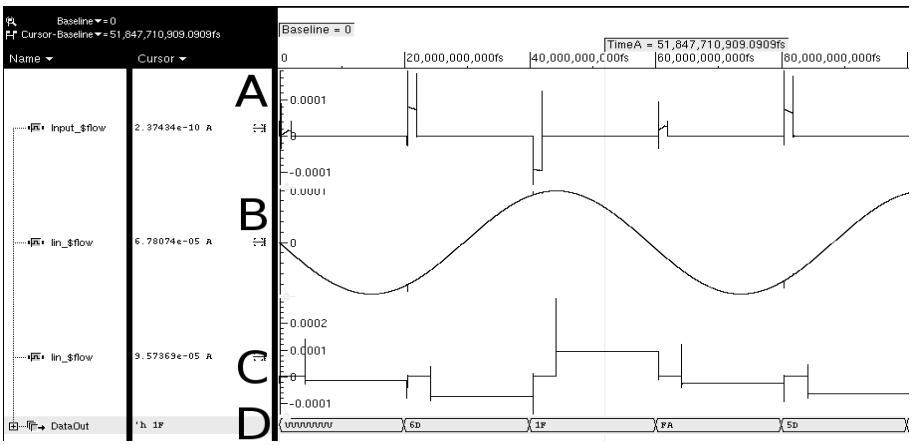

Figure 5. Mixed-signal simulation results.

5. CONCLUSIONS

The main objectives of this work were obtained since the ADC behavior followed the main specifications. The thermal behavior and the dynamic range of the ADC are under evaluation. To allow the acquisition of voltage signals, a voltage-to-current converter was also designed and shall be presented elsewhere. In the future, a more extensive characterization of the ADC shall be carried out.

6. ACKNOWLEDGMENTS

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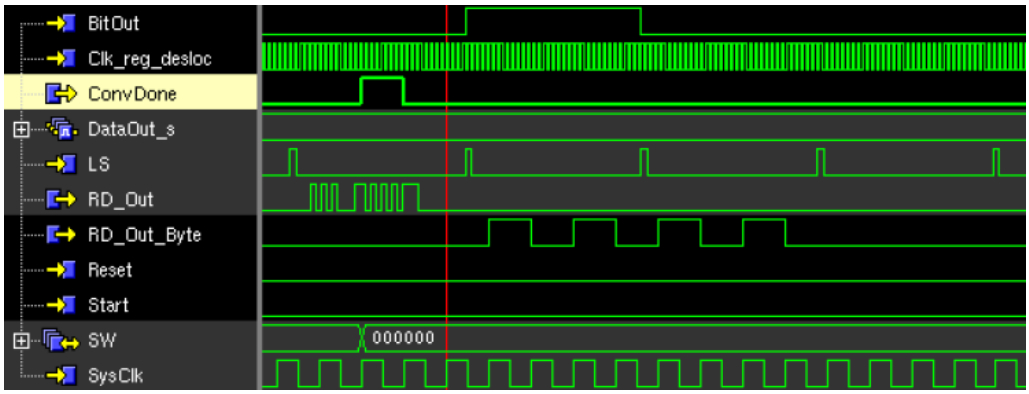

Figure 6. ADC digital core simulation results.

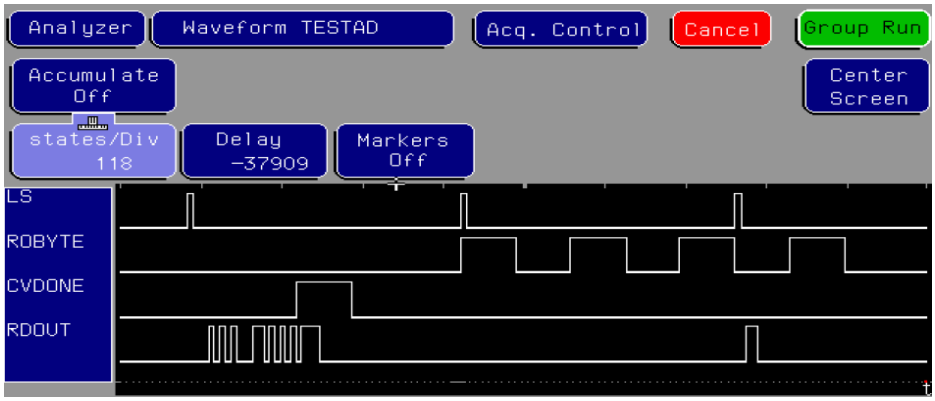

Figure 7. ADC digital core functional characterization.