Analog to Digital Converters Testing

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Abstract: Analog to digital converters (ADCs) are the front end of most of the modern measuring instruments. They affect crucially the interpretation of signals acquired from the real world into the digital domain. ADCs influence dominantly the accuracy of the instruments and limit their bandwidth. The exact ADC error description using standardized testing procedures are needed to evaluate instruments performance. This will be an important task for metrologists in the next future. The paper is aimed at providing a metrological overview of ADC testing.

Keywords: ADC, ADC testing, static test, histogram test.

1. INTRODUCTION

The block diagram of any digital measurement instrument includes Analog-to-Digital Converters after an analog conditioning block. The digital output from the ADC is usually processed in a digital signal processor according to the task to be performed. The analog front end presents a transfer characteristic similar to the stepwise characteristic of the ADC and it can be considered as a generalized AD converter.

Analog to Digital Converters are generally considered as ideal components affected only by quantization and timing errors. Real ADCs present however transfer characteristics that, depending on the input signal frequency and on the sampling rate, are in many cases far from the ideal ones, see figure 1.

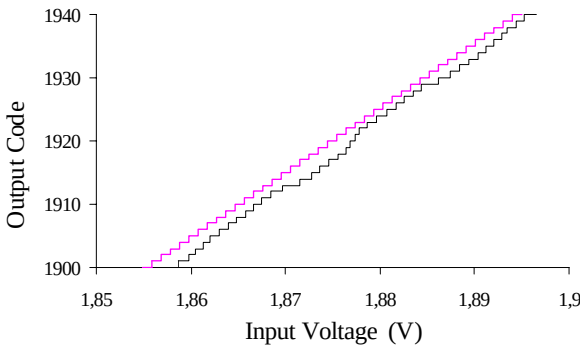

Fig. 1. Transfer characteristic of an ideal (black line) and of a real (light line) 12 bit ADC near middle scale.

2. ADC CHARACTERISTIC PARAMETERS

The main information about the ADC behaviour is contained in the vector of the transition code levels T(k). For each code bin value k the performance behaviour can be described by T(k), by the integral non linearity INL(k) or by the differential non linearity DNL(k) which are analytically linked [1-2]. Integral parameters describe by simple numbers the global metrological features of ADCs. Effective number of bits (ENOB) or signal to noise and distortion ratio (SINAD), are examples of this group of parameters. ADCs require for their complete characterisation an extremely high number of parameters; however end users usually take into account only some of them.

ADCs are traditionally tested as described in IEEE 1057 [1] and 1241 [2] standards. The development of new faster, cheaper and/or more accurate ADC testing procedures, able to characterize high resolution and high frequency converters has been one important task in measurement during the last decade.

The performance of the same converter under different conditions tends to vary, in some cases very strongly (Fig. 2). Consequently tests should be performed in conditions (input signal frequency and amplitude and sampling frequency) similar to those where they are expected to be used. Fig. 2 results show that ADCs performance limit not only the accuracy but also the bandwidth of the instruments where they are included.

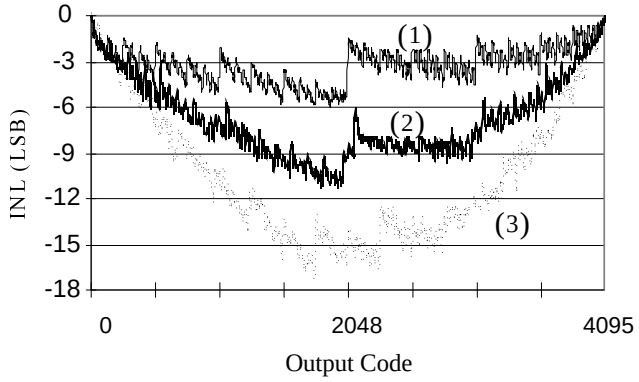

Fig. 2. INL of a 12 bit ADC, measured by the sinewave histogram test with a sampling frequency of 10 MHz and input sinewaves of 1 kHz(1), 20 kHz (2) and 60 kHz (3).

When the converters are to be used to acquire very low frequency signals, the static test is mandatory. In all other cases a dynamic test must be performed. Dynamic tests generally used can be divided in time domain, frequency domain and statistical domain tests. All test procedures present advantages and drawbacks. The main problem with the traditional static test procedure [1] is the unacceptable time duration of the tests for medium and high-resolution converters. The equipment required to test these converters with accuracy better than a small fraction of an LSB is also very expensive and consequently not available in many circumstances. Another problem is the inexistence of input stimulus sources to characterize state of the art very high resolution ADCs.

Regarding the traditional dynamic testing techniques, all of them are based on the use of "ideal" sinusoidal input stimulus (except in what concerns some time base tests). These ideal sources obviously do not exist and the validity of the approximation of considering them ideal will be lost when very high frequency or very high-resolution converters are under test. Other severe problem on these tests is the difficulty to assure coherent sampling in many cases.

3. THE STATIC TEST OF ADCS

Given the large number of low frequency application of ADCs, this is a very important test, both for the industry and the consumers.

Traditionally the test is performed as described in [1]. The transition levels are determined one at a time by applying a constant signal to the ADC input. The value of this stimulus signal is increased until it crosses each transition level, T(i). After each stimulus signal change a set of samples is acquired. The number of acquired samples depends on the standard deviation of noise in the experimental setup (σ_n) and on the required confidence and tolerance levels for the measurement. The value of each transition level is computed from the samples values and from the known values of the applied stimulus signal before and after transition level detection. This procedure is very time consuming because a high number of samples have to be acquired and processed. Furthermore it is necessary to wait for the output of the calibrator that generates the stimulus signal to settle each time it changes. This depends on the calibrator used but can go from a few milliseconds to more than one second. The duration of the test of a 12-bit converter can take several hours. If the sampling frequency is low, or the number of bits of the converter increases, the duration of the test becomes prohibitive. The calibrator used must have an output resolution lower than ¼ of the ideal quantization width, which implies the use of medium to high cost calibrators. The higher the resolution of the converter, the costlier is the equipment necessary.

The more recent IEEE 1241 standard [2], introduced a different procedure, in relation to IEEE 1057 std. it is based on the use of a feedback loop, where a DAC generates the feedback signal, applied to the ADC under test. The digital word input of the DAC, is incremented or decremented, depending on the result of the last ADC conversion. M measurements of the input signal of the ADC should be recorded in each step. M should be greater or equal to $2(\sigma_n/\varepsilon)^2$, where ε is the allowable code edge uncertainty. The number of samples to be acquired for each transition level depends on the step size, but it will be always greater than 9+M. All these samples are acquired at a rate that will be the smaller of the values of the settling time of the DAC and of the desired sampling period. If the settling time is high, the duration of the test will be prohibitive. It can be shown that this procedure is much faster than the static test described in [1] if the settling time of the DAC is low. It is a very good solution if dedicated hardware, containing a fast DAC, is to be used. However it should be avoided if a general-purpose calibrator with a large settling time is considered for ADC input signal generation. The procedure is particularly interesting for high-resolution, low sampling rate ADCs, since in this case the duration of the test is limited by the sampling rate, and the number of acquired samples in this procedure is very low.

A new test that allows the reduction of the test duration and on the possibility of the use of low cost equipment to perform the static test was recently developed [3-4] and included in the new IEC standard 62008 [5] and in the revision of IEEE 1057 standard [6]. It is based on the use of small amplitude triangular waves with variable DC levels as stimulus signal for the static test, see Fig. 3. This procedure is based in the traditional Histogram Method [7] but uses a uniformly distributed input signal that scans the ADC input range by increasing the DC level by steps.

The procedure requires several steps (N_s). In each step, a small number of ADC codes are stimulated repetitively via small triangular waves. The shape of the stimulus signal is always the same in every step, but the DC level is changed from step to step.

As in the traditional histogram test, the ADC is overdriven in order to stimulate all the codes and to exclude the samples corrupted by noise in the extremities of the stimulus signal [1]. In the case of a triangular stimulus signal, the samples in the extremity have to be excluded also to avoid distortions due to the discontinuity in the signal derivative.

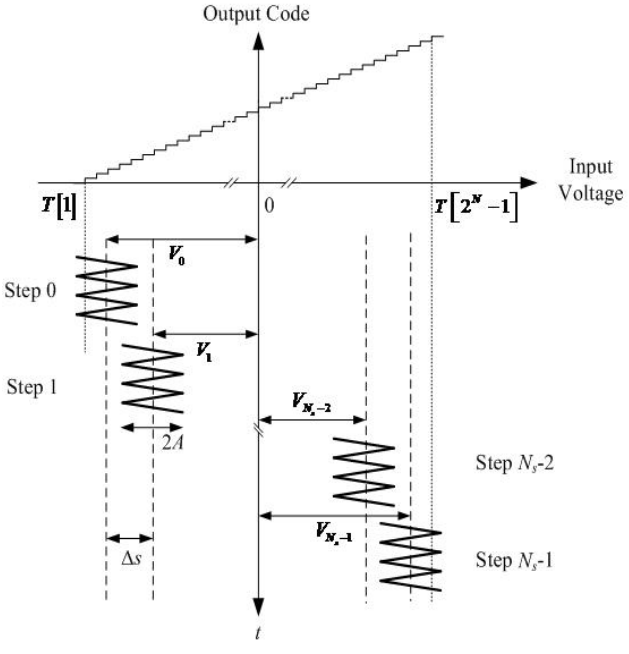

Fig. 3. Stimulus signal applied to the ADC in the new IEC 62008 and IEEE 1057-2007 standardised test.

For all the codes stimulated by each of the small triangular waves, the DNL is calculated according to the histogram test procedure. The transition levels are estimated from the DNL values. Gain and the offset errors are corrected, and the final DNL and the INL vectors are computed.

This new procedure for the static test of ADCs reduces dramatically the duration of the test and allows the use of low cost equipment. The time duration of the test is reduced because the number of changes in the DC level generator is dramatically reduced, 80 to 100 changes are the maximum number of changes needed in any ADC. In many cases, good results are achieved with a much lower number of steps. This means that for instance for a 12-bit ADC the waiting time for the calibrator to settle is reduced from 4×4096 to 80-100, i.e. a reduction of about 200 to 1! Another reason for the reduction of the test duration comes from the use of all acquired samples to compute all transition levels, it must be noted that in the traditional static tests [1-2] only a very small number of all acquired samples are actually used to determine the value of each transition level, and that after the computation of each level, all the previously acquired samples are discharged.

Fig. 4 presents the results of the traditional static test, performed as described in [1] for a 12 bit data acquisition board. The rms noise level of the experimental setup was estimated to be 0.2LSB. The acquisition of records with 4096 samples assures an accuracy of 0.012LSB for the INL.

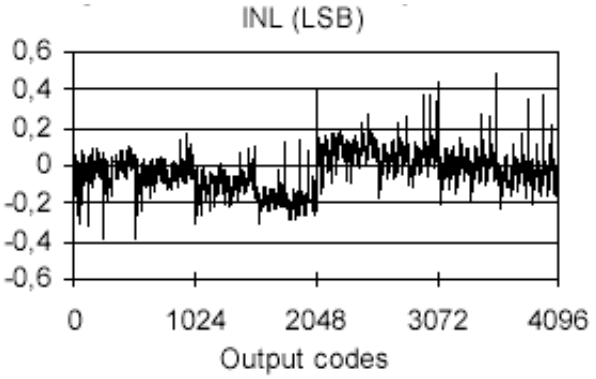

Fig. 4. Results of the IEEE 1057-94 standard static test of a 12-bit data acquisition board.

In [4] it was shown that a triangular generator with a poor nonlinearity was capable of performing the test if the input range is divided into a convenient number of intervals. A test was performed by acquiring a total of 20 million samples leading to an uncertainty in the INL results lower than 0.01LSB with 99.5% confidence. The difference between the results of the INL obtained with the histogram test and those obtained with the traditional static test ($\Delta INL = INL_{histogram\ test} - INL_{static\ test}$) is shown in Fig. 5.

The error introduced in the INL by the poor nonlinearity of the generator in the case of a full-scale triangular wave had a maximum value of 3.5LSB. It was reduced to 0.0175LSB as can be seen in the central part of the INLs difference (ΔINL) in Fig. 5. The higher values of ΔINL, in Fig. 5, for lower and higher codes are due to the decrease of accuracy of the traditional static test, due to the increase of the rms value of noise generated in the calibrator used as DC input stimulus, due to the change of its output circuitry for different output ranges. A significant reduction of the testing time in relation to the static test was achieved. The traditional static test in Fig. 4 took approximately 6 hours and the test with the new method took only about 5 minutes.

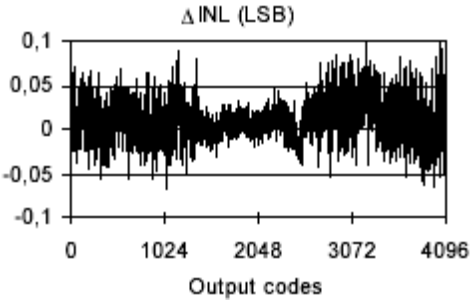

Fig. 5 INL difference of the small amplitude waves test results using 200 triangular waves and the traditional the static test results of Fig. 4.

The main drawback of this test arises from the acquisition of a small number of samples per period when the input signal frequency approaches the sampling frequency. This procedure is not, in its present form, suited for the dynamic test of ADCs since the small amplitude of the stimulus signal to use makes difficult the generation of a stimulus signal with sufficiently high slope to approach dynamic conditions.

4. DYNAMIC TEST OF ADCS

The histogram method [6-7] is the test procedure usually used to extract the dynamic transfer function of ADCs. It is based on the comparison of the known probability density function (pdf) of a repetitive dynamic input signal applied to the ADC and the distribution of codes at its output

Due to the practical difficulty of achieving economically accurate ramp or triangular wave generators, which would allow working with uniform pdfs, the sinusoid has become the stimulus signal for this test. The output codes distribution is compared with the theoretical sinusoid pdf, the DNL is computed and therefore INL and the transfer characteristic are derived. The equation traditionally used to compute the code transition levels in a sinewave histogram test is

$$T_{j+1} = O - A\cos\left(\pi \frac{HC_j}{M}\right), \qquad (1)$$

where A is the amplitude and O the offset of the input stimulus signal, HC_j the experimental cumulative histogram for code j and M the total number of acquired samples. Using (1), the accuracy on the evaluation of the code transition levels is “only” dependent of the spectral purity of the input sinewave and of the knowledge of its amplitude and offset.

Fig. 6 shows experimental results of the histogram test performed in a 12 bit ADC. It represents the number of occurrences of each code as a function of the digital output codes and consequently corresponds to trend of the sinusoid pdf, plus the influence of the ADC nonlinearity (which is what we want to measure) and the unwanted, but unavoidable influence of additive and phase noise, of the

finite number of acquired samples, of the incoherent sampling resulting from frequency errors between the input and sampling frequencies and from the lack of spectral purity in the supposedly sinusoidal input stimulus. From the results in Fig. 6 and the use of Eq. (1), one of the INL curves presented in Fig. 2 was computed and from this last the transfer function of fig. 1 was obtained.

In order to decrease the error induced by additive noise in transition levels determination, the input sinusoid must present an amplitude greater than the ADC end of scale limits [6-7]. This overdrive depends on the required tolerance and confidence levels for DNL and INL determination. The tolerance level (B) is measured in LSBs and the confidence level (v) is a probabilistic value. For transition code levels measurement they are related by

$$P\{T_t - BQ \le T_m \le T_t + BQ\} \ge 1 - v\,, \qquad (2)$$

where T_t and T_m stand respectively for the true and the measured values of the transition voltages.

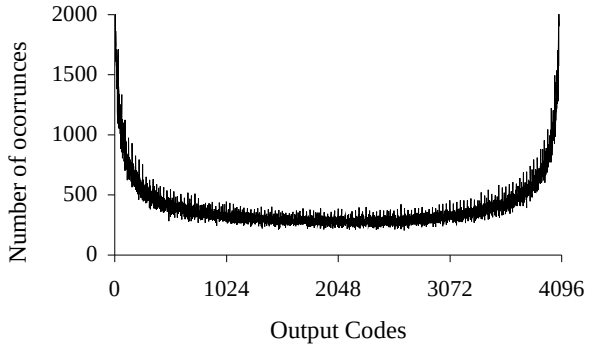

Fig. 6. Experimental results of a histogram test of a 12-bit *ADC* stimulated by a sinewave as described in [6], the total number of acquired samples was 1.7×10^6.

The total number of samples to be acquired during the histogram test depend on the noise level in the measurement system, on the required tolerance and confidence levels and is different if they are defined for DNL (quantization interval) or for INL (transition levels) determination. The number of samples depends also on the specification of tolerance for an individual transition level or code bin width, or for the worst case in all range. Expressions to compute the total number of samples and the amount of overdrive in the histogram test can be found in [6-7].

In any dynamic test of ADCs, stimulated by a sinusoid, the input signal frequency (f_{in}) must be selected in order to assure that for the chosen sampling frequency (f_s) the M acquired samples are uniformly distributed between 0 and 2π. This will happen if

$$f_{in} = \left(\frac{J}{M}\right) f_s\,, \qquad (3)$$

where J is an integer, prime in relation to M. This way M e J don't present any common factors and consequently exactly J periods of the input signal are contained in the M acquired samples. If M is a power of two, then any odd value for J meets the relatively-prime condition.

The accuracy required of the signal frequency depends very strongly on the frequency and depends also on whether the frequency deviation is in the positive or negative direction from the nominal value.

The use of a statistically defined electrical stimulus signal for the histogram test, like Gaussian noise, was proposed in [8-9]. When Gaussian noise is used as stimulus signal of the histogram test, code transition levels are computed through [9]

$$T_{i+1} = \sqrt{2}\sigma_R erf^{-1}(2HC_i - 1) + \mu_R\,, \qquad (4)$$

where σ_r and μ are the standard deviation and the mean of the noise stimulus and erf is the error function.

The standard deviation of the input noise to be used as stimulus signal in this test cannot be arbitrary for two reasons: (i) it must be such as to excite all levels of the converter; (ii) as shown in [8], an optimum value exists that minimizes the required number of samples for a given pair of tolerance/confidence (B/v) levels in the measurement of INL and DNL vectors. In [8] an expression for the number of required samples was derived.

The use of Gaussian noise as stimulus signal presents the following advantages:

(i) only the first order statistics are relevant for the characterization; (ii) a noise wave is as easy as or easier to generate than a sine wave, especially when high resolution or high frequency converters are under test; (iii) noise in the test ensemble will only add its variance to the noise of the generator, as long as both possess normal distribution; (iv) noise is not periodic, thus not requiring hard to implement sampling schemes. Apart from that, the use of Gaussian noise should be considered in those cases where the ADC is expected to acquire signal with a pdf similar to that of random noise. It is the case for instance of audio signals. Converters for use in digital radio or on modern digital communication systems should be tested with such a stimulus. It is well know that ADCs exhibits in many cases nonlinearities dependent of the input signal pdf as a consequence of localised heating effects in ADC integrated circuits, the use of a sinusoidal wave as input signal for the test, with pdf maximums in the input range limits will lead to different results of those obtained with waves presenting pdf maximums in the central part of the range.

Caution must be taken in order to avoid device damage by high input signal amplitude when this stimulus signal is used. In fact, due to the nature of normal distributed noise, a high variance implies the existence of a finite probability for the occurrence of potentially damaging levels. Consequently, a limiting circuit must be included (except in the cases where noise is originated in a pseudo-random digital sequence) that does not distort the input signal normal pdf within all the input ADC range.

DFT and sine fitting tests are used in fast dynamic tests of ADCs. Traditionally they are used to measure noise, signal to noise and distortion ratio and ENOB [1-2, 10]. More recently they were proposed to obtain the INL, the DNL and the transfer function of ADCs, namely when they present a hysteric behaviour [11-13].

5. CONCLUSION

The paper presented a metrological overview of ADC testing. The reader interested in the field is invited to visit the bibliographic references.

Tenths of scientific works were presented in the last decade in this field. However, the metrological characterisation of ADCs and DACs is not feasible on national or private level. In fact, metrology is always a global task, and relevant organisations like IMEKO and IEEE aware of the need to carry out research activities in the digitising field did a significant contribution in the recent past. The International Measurement Confederation (IMEKO) is devoted to metrology and measurement with worldwide membership. Inside IMEKO TC-4 a network was formed under the name EUPAS, European Project for ADC-based devices Standardization, and which extends over about 20 institutes within 14 European countries (Czech Republic, Estonia, Finland, France, Germany, Hungary, Italy, Poland, Portugal, Russia, Slovak Republic, Spain, UK, Ukraine). The aim of this project was to improve existing standards for quality control of ADC-based embedded systems, making components and products interchangeable and to simplify test procedures.

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