NEW JITTER MEASUREMENT TECHNIQUE USING TDC PRINCIPLE IN A FPGA COMPONENT

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Abstract: The paper presents a new approach for measure and analysis of jitter. The measures are made with the Time to Digital Converters with an electronic implementation that uses VHDL language in a FPGA component. The electronic system data are registered and processed by software that to extract the necessary parameters to characterize this effect in a communication systems.

Key words: Time jitter measurements, Time to Digital Converters.

1. INTRODUCTION

Time jitter is an undesirable effect appearing in electrical systems that use voltage transitions to represent time information. The main consequences are in errors introduced in the reading of time intervals, in the recovery of clock and in identification of symbols used in digital communications.

There are various criteria to measure time jitter is a waveform, known as period-jitter, cycle-cycle jitter, time interval error (TIE), as shown in Figure 1.

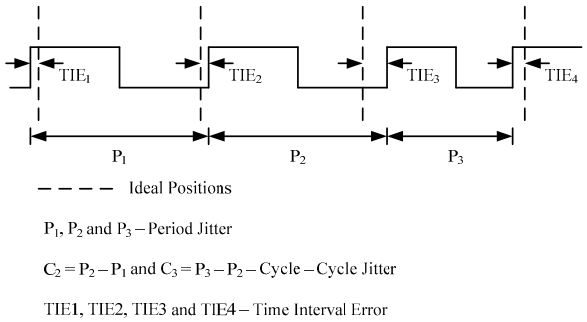

Fig. 1. Criteria to measure time jitter

The cycle-cycle jitter can be obtained from the difference between successive jitter periods. The TIE can be determined from the integration of the jitter period after being subtracted from each nominal clock period.

Time variations are conventionally classified in two categories as a function of time, known as jitter and wander, corresponding to the *short-term* and the *long-term* variations of the significant instants of a digital signal from their ideal positions in time, respectively. The two categories are separated by the threshold frequency of 10 Hz as defined by the International Telecommunication Union, ITU [1].

Most of wander time shifts in serial communication links do not bring serious consequences, since they are efficiently eliminated by the clock recovery circuits.

1. JITTER MEASUREMENTS AND ANALYSIS

The time jitter can be measured by a storage oscilloscope, as seen in Figure 2. It contains various waveform periods stored, with the accumulation of transitions compared to the ideal detection position. The time width corresponds to the TIE.

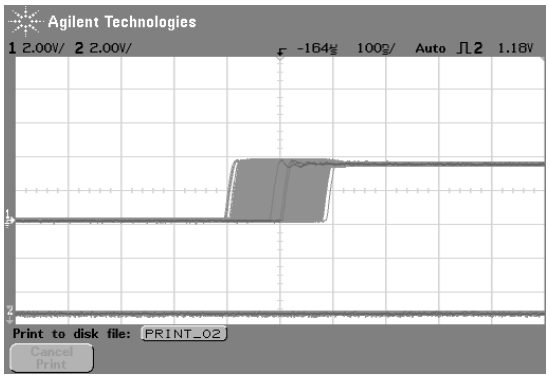

Fig. 2. TIE measurement using a storage oscilloscope.

However, this measurement does not describe entirely the nature and the causes that produce the

jitter effect. The non-deterministic jitter component can be analyzed statistically.

The jitter can be decomposed as proposed in Figure 3. It is possible to associate different jitter component to a particular physical effect. This can be useful in the search of their generation in the system.

The random jitter (RJ) component cannot be predicted. In most cases it has a gaussian nature. It is produced by the noise from the power supply sources and phase noise produced by frequency converters. It is the most common in telecommunication radio links as well as to the current application.

The deterministic jitter components are characterized by their repetition rates and periodicities. It is classified in periodic jitter (PJ), data-dependent jitter (DDJ) and duty-cycle jitter (DCD).

The PJ is typically caused by an external deterministic interference cause. Among the possibilities are the spurious signals generated by power supply sources; interferences caused by RF carriers, and by unstable clock recovery PLL circuits.

The DDJ is related to a sequence of bits in a data stream. It is caused by the dispersion in frequency response in cables and components in the system.

The DCD is the result from transition time interval changes caused by components that offer different slew rate for the rising and falling edges [2][3].

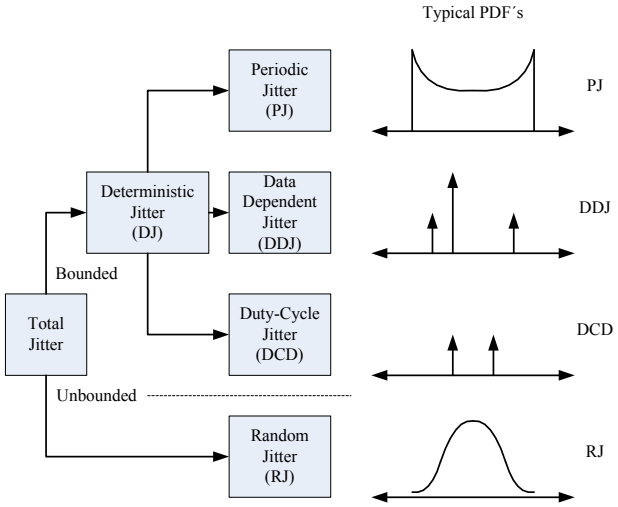

Fig. 3. Diagram showing the jitter decomposition.

2. JITTER MEASUREMENT WITH TDC TECHNIQUE

There are a number of instruments used to measure jitter in the fields of telecommunications (optical and electrical), electronics and computers. They derive the parameters necessary for the analysis of their effects in the systems.

We present here a low-cost solution for jitter measurements, using components operating at low processing frequencies, while assuring highly performing accuracy and precision.

The proposed technique requires a stable and reliable electronic platform, being selected a VHDL (VHSIC Hardware Description Language) in a FPGA (Field Programmable Gate Array) component.

The electronic board delivers the data through a serial interface to a micro-computer. The data are analyzed by appropriate softwares. The structural block diagram is shown in Figure 4.

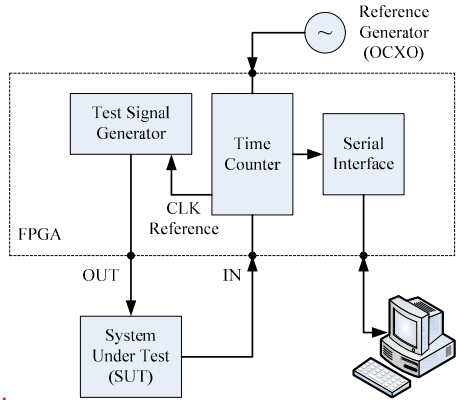

Fig. 4. Block diagram of the measuring system.

The FPGA component generates the test signals applied on the system under test (SUT). The signal goes into the SUT and is received by the FPGA component that measures the jitter, delivering it to the computer. The data analysis software produce the jitter numerical parameters and graphic representation.

Different techniques can be used for time count, such as: time to digital converters (TDC); vernier; pulse overlap and the start-stop principle.

We selected the TDC technique for its precision using digital components such as the FPGA. The simpler and direct time count method is based on start and stop pulses. However this method requires high clock frequencies to obtain better accuracies.

Keeping the start-stop concept, it possible to count time using a clock and generating *N* signals at the same frequency, but phase shifted in time. Thus the count resolution will depend not only on the clock frequency, but also on the number of waveforms. The phase shift between *N* signals will define the resolution of the measuring system. Therefore it is possible to assemble a system exhibiting high time resolution using low frequency clock.

The OCXO phase noise is not taken into account, because the system refers to the same frequency reference.

3. TDC TECHNIQUE IMPLEMENTATION

The time measurements using the TDC technique is based in delay lines and interpolation circuits, which may produce interpolation errors[4-6].

The system presented here utilizes a number of counters equal to the number of phase shifted outputs to obtain the partial counts without interpolation errors.

All elements are in a single chip under the same temperature and bias conditions

The *N* phase shifted outputs (Figure 5) produce waveforms displaced in time from each other by a small interval Δ_t.

The *N* phase shifted waveforms are described by VHDL resulting in hardware implementation in a FPGA tool. It is possible to measure the time difference Δ_t between successive waveform rise transitions, which correspond to the minimum measurable time interval, or the clock reading accuracy.

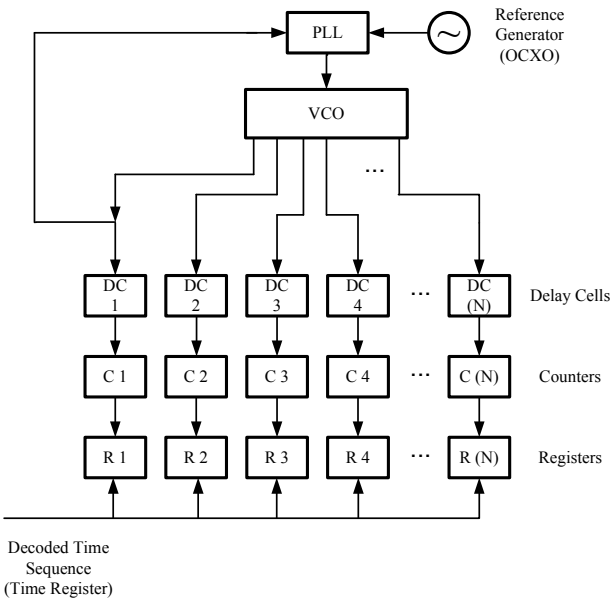

Fig. 5. TDC technique Block Diagram [7].

The phase shift between waveforms progresses linearly, such as:

$$\begin{aligned} D_{1-2} &= \Delta_t \\ D_{1-3} &= 2 \cdot \Delta_t \\ &\vdots \\ D_{1-N} &= (N-1) \cdot \Delta_t \end{aligned} \qquad (1)$$

where $D_{1\text{-}2}$ is the phase shift between waveforms 1 and 2, $D_{1\text{-}3}$ between waveforms 1 and 3 and so on, until $D_{1\text{-}N}$ for the last waveform. As the counters' registers change as a function of the waveform rise transition fed in, these transitions are represented in Figure 6 by $TR_{m,N}$ where *m* is the transition number and *N* the respective counter number. The relationship between the number of counters and the phase shift between waveform rise time transitions is as follows:

$$\Delta_t = \left(\frac{T_C}{N}\right) = \left(\frac{1}{N \cdot F_C}\right) \qquad (2)$$

where F_C is the FPGA operating frequency, related to the number of counters needed to obtain a given accuracy.

In Figure 6, the decoded time sequence (time register) triggers the clock reading. In this example the time register in on waveform transition 4 for the first counter, which means a time reading equal to $4\,T_C$. The reading accuracy is improved taking a Δ_t increment for each counter forwhich the time register remains at the same waveform transition as the first counter. In this example, the accurate reading become $4\,T_C + \Delta_t$. We can express the time measured by the general equation:

$$Time = \left(TR_{m,1} \cdot T_C\right) + \sum_{i=2}^{N} \left(B_i \cdot \Delta_t\right) \qquad (3)$$

where *m* is the transition number, index *i* is the counter number (varying from 2 to N). Factor *B =1* when *i* is the same as counter number 1, and *B=0* when *i* is different from counter number 1.

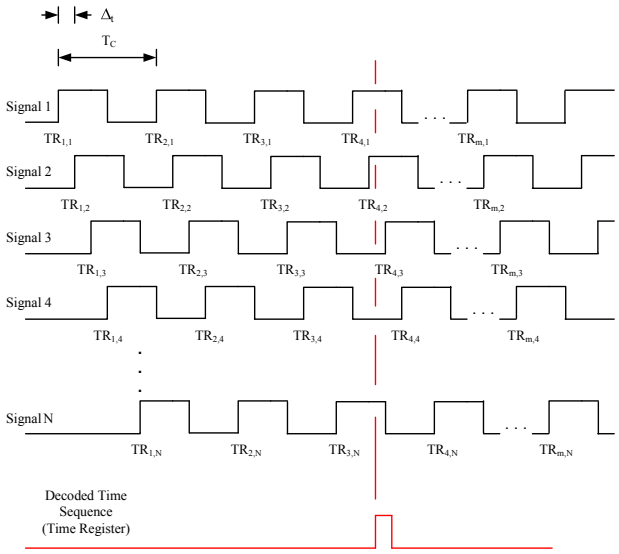

Fig. 6. TDC technique waveforms [7].

3. RESULTS

We present the time count and jitter measurements using the TDC technique, processed by Matlab software routines, in a wireless radio telecommunication link, used in the Geolocal new positioning system [8][9].

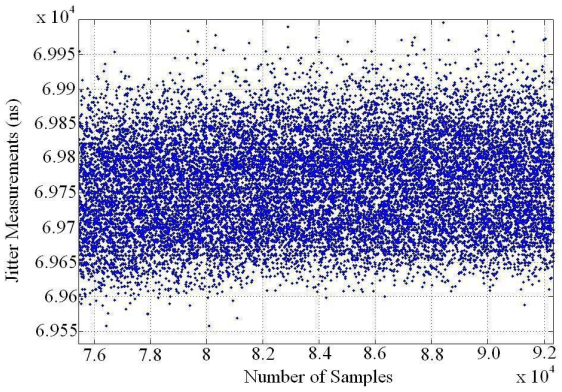

Fig. 7. Jitter measurements with time.

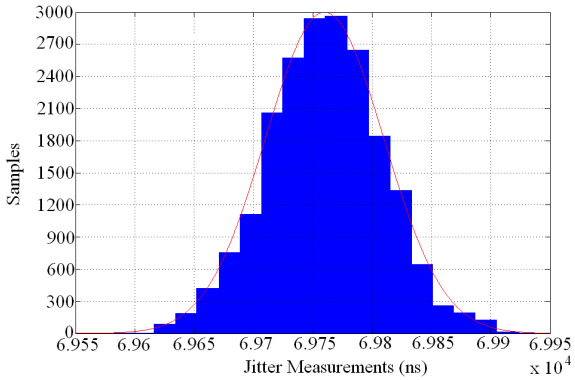

Fig. 8. Jitter distribution histogram

The results are shown in Figure 7, for measurements taken along a time scale of 4h 26.7m. The jitter peak-to-peak range is of about 353 ns. The jitter distribution is shown in Figure 8. It fits approximately a gaussian function with 202 ns RMS variations.

The technique shown here allows jitter measurements using data obtained with reliable 1 ns resolution. It requires low cost components, and use flexible software processing. Higher accuracies, of the order of tens of picoseconds, can be obtained with the use of more sophisticated FPGA components.

4. ACKNOWLEDGMENTS

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REFERENCES

[1] ITU-T Recommendation G.810 (08/96) “Definitions and Terminology for Synchronization Networks”

[2] Papoulis, A.; Pillai, S. U.; Probability, Random Variables and Stochastic Processes ; 4th Ed. Mc Graw Hill; 2002.

[3] Jr. Davenport, W. B.; Root, W. L.; An Introduction to the Theory of Random Signals and Noise; IEEE Press; 1987.

[4] D.I. Porat, “Review of sub-nanosecond time-interval measurements”, *IEEE Trans. On Nucl.Sci.* **NS-20**, 36-51, 1976.

[5] J. Kalisz, “Review of methods for time interval measurements with picosecond resolution”, *Metrologia* **41**, 17-32, 2004.

[6] R. Pelka, “Nonlinearity correction on the integrated time-to-digital converter with direct coding”, *IEEE Trans.Instrum. and Measurement* **46**, 449-453, 1997.

[7] C.N.M. Marins, P. Kaufmann, A.A. Ferreira Jr., P.H. Lopes, M.C. de Paiva, R.M. Villela and A.C. Silveira, “Precison clock and time transfer on a wireless telecommunication link”, submitted, 2008.

[8] P. L. Kaufmann *et al.,* "Non recursive algorithm for remote geolocation using ranging measurements", *Math. Problems in Engineering*, v. 2006, pp. 1-9, Article ID79389, DOI:10.1155/MPE/2006/79389,2006

[9] “Geographic and space positioning system and process”, Brazil Patent PI 03003968-4, Filed 08.10.2003, and International Patent Cooperation Treaty PCT/BR2004/000190, Filed 04.10.2004.